Columbia University
Department of Electrical Engineering
Solid State Devices and Materials
ELEN E3106
Homework #9

Due: Monday, December 8th by 11:59pm
Goal: The purpose of this exercise is to help you review the basic theory of the MOSFET, introduce you to some key device parameters, and give you a feel for the typical values of key device performance metrics for state-of-the-art MOSFETs.
Instructions: For problems 1 and 2 below, you will need to run the simulation program, nano-CMOS, on nanoHUB.org. Be sure you have an account, then proceed with the exercises below. Locate the simulation tool, nano-CMOS (https://nanohub.org/tools/nanocmos), and use it to examine the I-V characteristics of CMOS technology. You should clearly describe how you obtain each parameter. Note that you are able to change the minimum and maximum axes scales and to select either linear or logarithmic scales.
Points: 110 for 3106 and 130 for 4106

- **Problem 1 (27 pts)** (Lundstrom) Select "NMOS 32nm," and use the default values. Push the "Simulate" button, and then answer the following questions.
  (a) What is the on-current (taken at $V_{gs} = V_{ds} = V_{DD} > V_t$) in $\mu A/\mu m$?
  (b) What is the off-current in $\mu A/\mu m$?
  (c) What is the subthreshold swing, S, in mV/decade? Note, decade means a factor of 10 increase in I_d.
  (d) Estimate $V_{d,sat}$ for $V_{gs} = 0.9\,V$. Don't eyeball the answer, make sure to develop a simple methodology. You may annotate the plots for this.
  (e) Estimate the DIBL in mV/V.
  (f) Estimate the threshold for both $V_{ds} = 0.9\,V,\ 0.09\,V$. Which one represents the linear regime? Which one represents the saturation regime?
  (g) Estimate the output resistance, r_0, in $\Omega - \mu m$ for $V_{gs} = V_{DD}$.
  (h) Estimate the **approximate** channel resistance, $R_{channel}$, in $\Omega - \mu m$ as the resistance in the linear region for the maximum gate voltage. In reality, the total device resistance from source to drain is the sum of the channel resistance and source and drain resistances as we will see in Problem 5.
  (i) Estimate the transconductance g_m, in mS/mm at the maximum gate (and drain) voltage.

- **Problem 2 (27 pts, 3 pts each)** (Lundstrom) Repeat problem 1 for a p-channel MOSFET by selecting "PMOS 32nm," and use the default values. Push the "Simulate" button, and then answer parts (a-i). Discuss the main differences that you see.

- **Problem 3 (20 pts, 5 pts each)** Classic pMOSFET. (Howe HW 7)

A silicon pMOSFET is fabricated with substrate doping $N_d = 6 \times 10^{17}\ cm^{-3}$. The gate oxide is SiO_2 with t_{ox} = 5 nm. Assume a well-behaved, long-channel device with L = 1 μm, W = 4 μm, and hole mobility 200 $cm^2V^{-1}s^{-1}$.

(a) Explain why the hole mobility is lower in the channel than in bulk silicon.

(b) Find the V_t of the pMOSFET when n+ poly-Si is used to fabricate the gate electrode. (You may assume $E_F \approx E_C$ for degenerately doped n+ silicon.)

For part (c) and (d), note the following: You must use a modified version of our drain current equation in the linear regime in order to get a smooth curve: $I_d = \frac{W}{L}\mu_p C_{ox}(V_{gs} - V_t - \frac{V_{ds}}{2})V_{ds}$. Assume $I_d = 0$ in cut-off.

(c) Numerically plot the $|I_d|\ vs.\ V_{gs}$ curve from V_{gs} = -3 to 0, and V_{ds} = -0.1 V.

(d) Numerically plot the $|I_d|\ vs.\ V_{ds}$ curve from V_{ds} = -3 to 0, and V_{gs} = -3 V.

- **Problem 4 (24 pts, 4 pts each)** Output characteristics of an nMOSFET (Howe HW 7)

The $I_d - V_{ds}$ characteristics and dimensions of an n-channel MOSFET are shown below. Please estimate the drift velocities of electrons at the source and drain, respectively, at the points given below. Hint: $I_d = WQ_{inv}v$ and you may assume that $E_{sat} \approx 3\times10^4\ V/cm$ and $v_{sat} = 10^7\ cm/s$. Use the following numbers in your calculations:

A: $I_{ds} = 1.5$ mA $V_{ds} = 0.5$ V

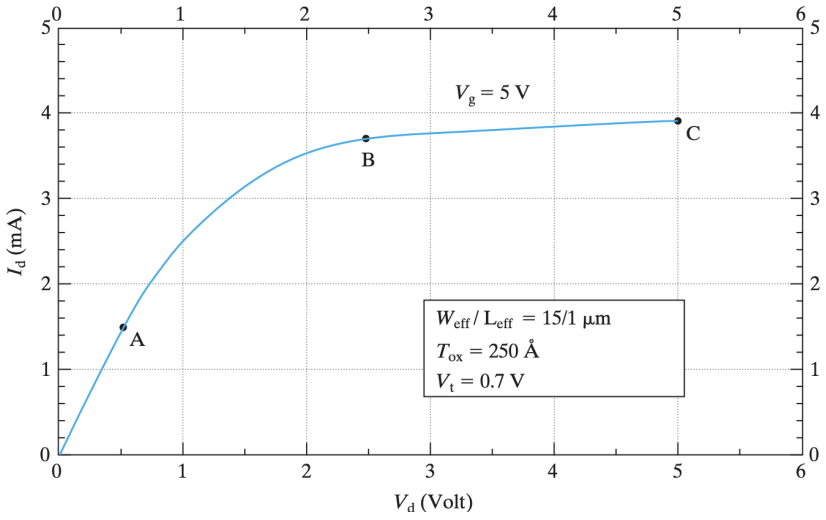
B: $I_{ds} = 3.75$ mA $V_{ds} = 2.5$ V

C: $I_{ds} = 4.0$ mA $V_{ds} = 5.0$ V

(a) At point A

(b) At point B

(c) At point C



- **Problem 5 (12 pts, 6 pts each)** Effect of parasitic series resistance on MOSFET operation.

So far, we have neglected the parasitic series resistances in MOSFETs, but real devices have source and drain series resistances, R_S and R_D, respectively. The total resistance across the source and drain contacts is then $R_S + R_{channel} + R_D$. Assume that V_{ds} is very low in this problem.

(a) Write down an expression for $R_{channel}$ which depends on V_{gs} (Hint: $R_{channel} = V_{ds}/I_{ds}$). Given t_{ox} = 3 nm, W/L = 1/0.1 μm, $V_{gs} = 1.5\,V$ and $V_t = 0.4\,V$,what is I_{dsat} for $R_s = 0,\ 100,$ and $1,000\ \Omega$? Assume that we observe no obvious short channel effects on the device (e.g. use the square law approximation). The drain saturation current is given,

$$I_{dsat} = \frac{I_{dsat0}}{1+\frac{I_{dsat0}R_S}{V_{gs}-V_t}}$$

- **Problem 6 (REQUIRED FOR 4106 students only) (20 pts, 4 each)** Effect of body bias on MOSFET parameters.

Consider a state-of-the-art deep-submicron n-channel MOSFET. Indicate the impact of applying a back bias, $V_{sb} > 0$ (voltage between the source and body), on the parameters and figures of merit (FOM) listed below. Nothing else is changed. Check the box that corresponds for each item (increase, decrease, or no effect). Give the reason for your choice.

Parameter/FOM	**Increase**	**Decrease**	**No effect**
Threshold voltage, V_t			
Subthreshold slope, S (in mV/dec)			
DIBL			
Effective inversion layer mobility at a given V_{gs}, μ_{eff}			
Drain current for $V_{gs} = V_{ds} = V_{DD} > V_t$, I_{on}			